What is Claimed is:

1. A metal oxide semiconductor (MOS) device comprising:

a semi-conducting substrate having source and drain regions;

a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate; and

a gate formed of a metal selected from the group consisting of Re, Rh, Ir, Pt and Ru on top of said gate dielectric layer.

2. A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer having a thickness of less than 50 Å.

3. A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

4. A metal oxide semiconductor device according to claim 1, wherein said gate dielectric layer is formed of a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

5. A metal oxide semiconductor device according to claim 1, wherein said dielectric layer is formed of SiO_2.

6. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate has at least one source and one drain region.

7. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is p-type or n-type.

8. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

9. A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of silicon.

10. A field effect transistor (FET) comprising:

a semi-conducting substrate having at least one source and one drain region;

a gate dielectric layer of less than 100 Å thickness on the semi-conducting substrate; and

a gate formed of a metal selected from the group consisting of Re, Rh, Ir, Pt and Ru on top of the gate dielectric layer.

11. A field effect transistor according to claim 10, wherein the gate dielectric layer has a thickness of less than 50 Å.

12. A field effect transistor according to claim 10, wherein said gate dielectric layer is formed of a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

13. A field effect transistor according to claim 10, wherein said gate dielectric layer is formed of a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

14. A field effect transistor according to claim 10, wherein said semi-conducting substrate is p-type or n-type.

15. A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs and organic semiconductors.

16. A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of silicon and said gate dielectric layer is SiO_2.

17. A method for forming a metal contact in a semiconductor device comprising the steps of:

depositing a dielectric material layer of less than 100 Å thickness on an active surface of a pre-processed semi-conducting substrate;

depositing a layer of metal selected from the group consisting of Re, Rh, Pt, Ir and Ru by a chemical vapor deposition method;

patterning said metal layer and forming a metal electrode on said dielectric layer; and

passivating said metal electrode and said dielectric layer in forming gas.

18. A method for forming a metal contact in a semiconductor device according to claim 17 further comprising the step of depositing said dielectric layer by a material selected from the group consisting of SiO_2, nitrided SiO_2, Si_3N_4, metal oxides and mixtures thereof.

19. A method for forming a metal contact in a semiconductor device according to claim 17 further comprising the step of depositing said dielectric material layer in a thickness less than 50 Å.

20. A method for forming a metal contact in a semiconductor device according to claim 17 further comprising the step of depositing said dielectric material layer by a material selected from the group consisting of Al_2O_3, HfO_2, ZrO_3, Y_2O_3, La_2O_3 and mixtures thereof including silicates and nitrogen additions.

21. A method for forming a metal contact in a semiconductor device according to claim 17 further comprising the step of depositing a metal layer of Re by using $Re_2(CO)_{10}$ as a source material by said chemical vapor deposition method.

22. A method for forming a metal contact in a semiconductor device according to claim 17 further comprising the step of passivating said metal electrode and said dielectric material layer by annealing in forming gas.

23. A method for forming a metal contact in a semiconductor device according to claim 17 further comprising the step of depositing said metal layer in a substantially uniform thickness, having a thickness variation of less than 10% across said semi-conducting substrate.